Single Chip Ka-Band Transceiver

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Abstract

This paper presents the first monolithic single chip FM-CW radar transceiver operating at 40 GHz. The chip is the largest multifunction MMIC demonstrated operating at millimeter-wave frequencies. The design implements transmitter receiver, and duplexer functions using a single process InGaAs HEMT technology. The transmitter operates in the frequency range from 37 to 40 GHz and has greater than 12.0 dBm output power. The receiver converts the signals in the same frequency range to an IF frequency of 10 to 100 MHz with 0 dB conversion loss. When integrated with an antenna, the chip is a fully functional FM-CW radar which detects the doppler frequency shift from reflected objects. The paper will describe the design, fabrication, and performance of the chip.

Introduction

The need to develop integrated multifunction circuits at millimeter-wave frequencies is rapidly increasing. Although high performance receiver and transmitter components fabricated using conventional waveguide or hybrid integrated circuit structures have been demonstrated at millimeter wave frequencies, the use of these components in radar systems is often hampered by the excessive expense incurred in the fabrication of precision machined parts, and labor intensive assembly of the waveguide and the hybrid integrated circuit structures. Reducing the cost, size, and weight of these components by monolithic implemention at millimeter frequencies can be an advantage[1][2]. In this paper we describe the design, fabrication and evaluation of the single chip Ka-band transceiver. This result represents the highest degree of integration achieved for an FM-CW radar application at 40 GHz.

Design

The transceiver consists of 7 active microcells: VCO, buffer amplifier, power amplifier, low noise amplifier, single balanced mixer, voltage controlled phase shifter, and attenuator. Figure 1 shows the block diagram of the transceiver circuit. The details of the circuit design, development, and evaluation are presented below.

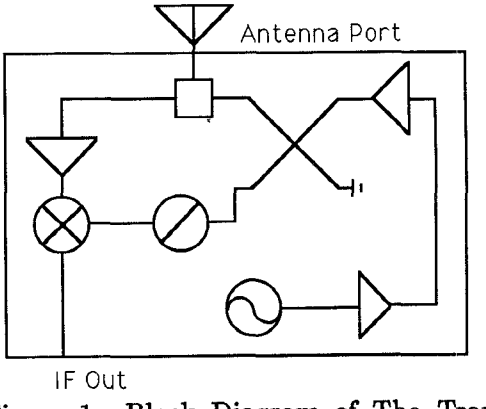

Figure 1: Block Diagram of The Tranceiver.

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Transmitter

The objective of the tranmitter was to achieve 17 dBm of output power at 37 GHz. The transmitter contains the VCO, two stage buffer amplifier, and two stage power amplifier.

The local oscillator is a critical component in the design of the transmitter because it determines the operating frequency and output power of the transceiver. It was designed to provide 3 dBm of output power and can be tuned though the source or gate tank circuits. The measured response of the oscillator circuit, shown in Figure 2, indicated a tunning range from 37.6 GHz to 39.4 GHz with an output power of 3 to 5 dbm.

The buffer amplifier was to designed to provide 10 dB of gain from 33 to 38 GHz. The design approach chosen for the buffer amplifier utilized bandpass matching topologies for the input, output and interstage matching networks. The buffer amplifier had a measured gain of 13 dB from 33 to 38 GHz as shown in Figure 3.

The design approach for the power amplifier was chosen to allow the integration of power and receiver functions on a single monolithic substrate. The objective of the power amplifier was to provide 10 dB of gain and 17 dBm output power from 33 to 38 GHz. The measured data indicated the power amplifier acheived 12 dB of gain with 18 dBm of saturated output power from 33 to 40 GHz. The measured response of the power amplifier is shown in Figure 4; the measured output power is shown in Figure 5.

Receiver

The objective of the receiver design was to convert the doppler shifted input signals from Ka-band to an IF frequency range of 10 to 100 MHz with a conversion loss of 0 dB and a noise figure of 9 dB. The measured conversion loss of the receiver was 0 dB. The receiver contains a two stage LNA and single balanced HEMT mixer. The measured conversion loss of the receiver is shown in Figure 6.

The design objective of the LNA was to provide 9 dB of gain from 33 to 38 GHz with a 7 dB noise figure. The low noise amplifier utilized bandpass topologies for the input output and interstage matching networks. The low noise amplifier achieved 13 dB of gain with a 6.5 dB noise figure from 34 to 38 GHz. The measured response of the low noise amplifier is shown in Figure 7.

The design objective for the mixer was to provide 8 dB of conversion loss and 8 dB noise figure from 33 to 38 GHz, with an IF frequency of 10 to 100 MHz. The design topology chosen for the single balanced mixer incorporated a rat-race ring hybrid and two HEMTs connected in cascode configuration to form the balanced mixer. The output of the mixer is a low pass filter which terminates the RF and LO frequencies. The performance of the mixer improved as the LO drive level increased to saturate the mixer at 9 dBm. The measured conversion loss of the mixer was 5 dB from 10 to 100 MHz as shown in Figure 8.

Transceiver Results

The transceiver circuit was fabricated on In-GaAs/GaAs psuedomorphic material, which was grown with MBE. The circuit was processed using the TRW base line planar HEMT process[2]. The transceiver chip illustrated in Figure 9 measured 4.35 MM X 7.0 MM. The receiver had a measured conversion loss of 0 dB at 38 GHz. The transmitted output power of the transceiver measured +12 dBm at 38 GHz. The measured response of the transceiver is shown in Figure 10.

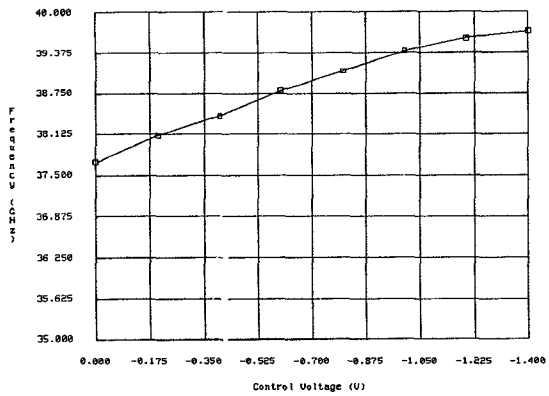

Figure 2: Measured Response of Oscillator Circuit.

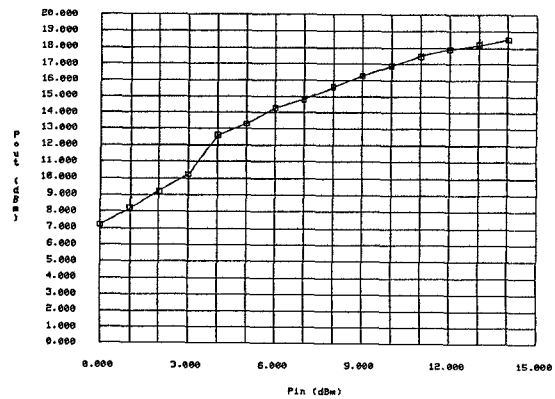

Figure 5: Measured Output Power of Power Amplifier.

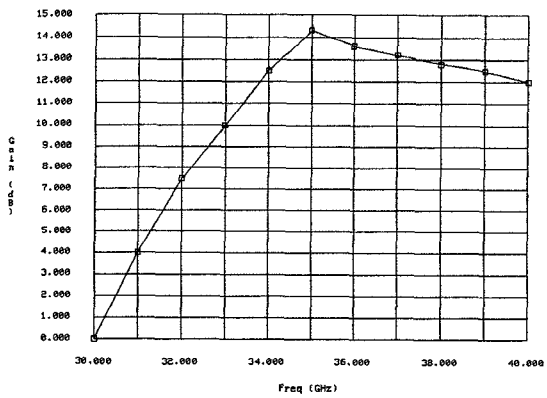

Figure 3: Measured Response of Buffer Amplifier.

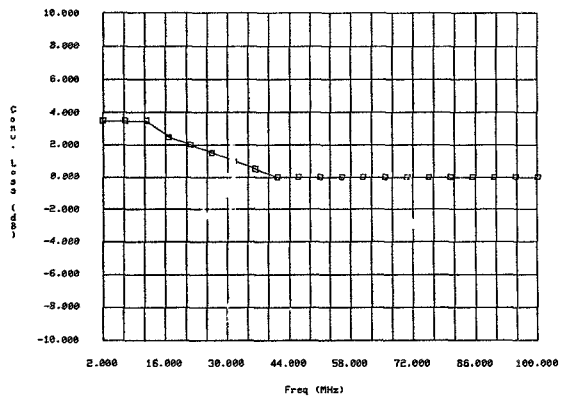

Figure 6: Measured Conversion Loss of Receiver.

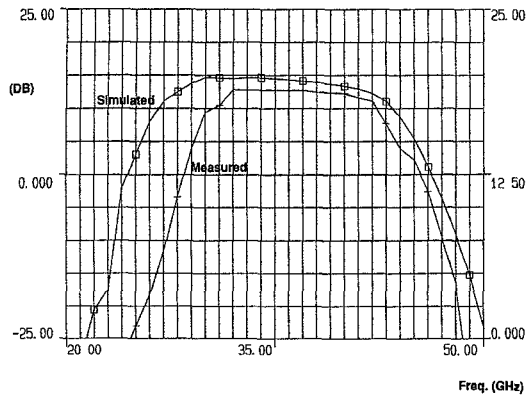

Figure 4: Measured Frequency Response of Power Amplifier.

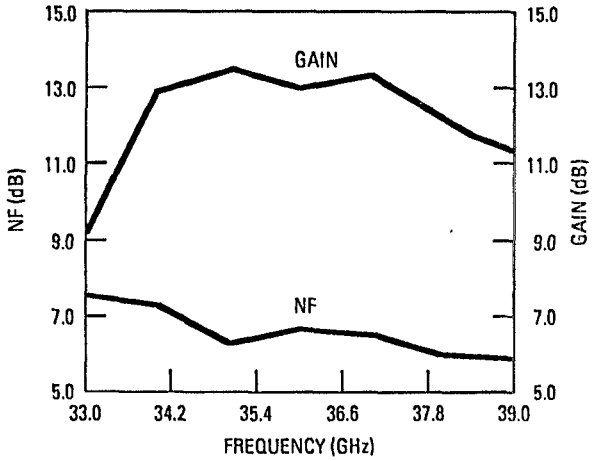

Figure 7: Measured Response of Low Noise Amplifier.

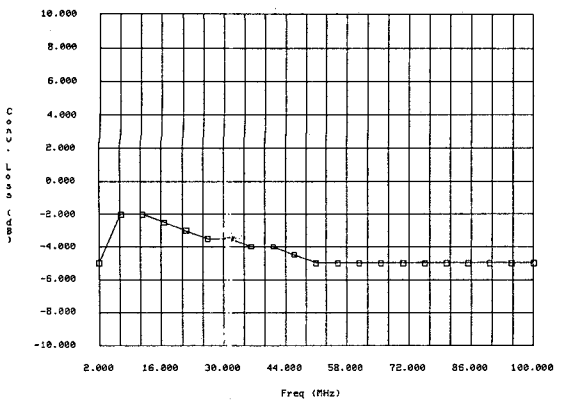

Figure 8: Measured Response of Single Balanced Mixer.

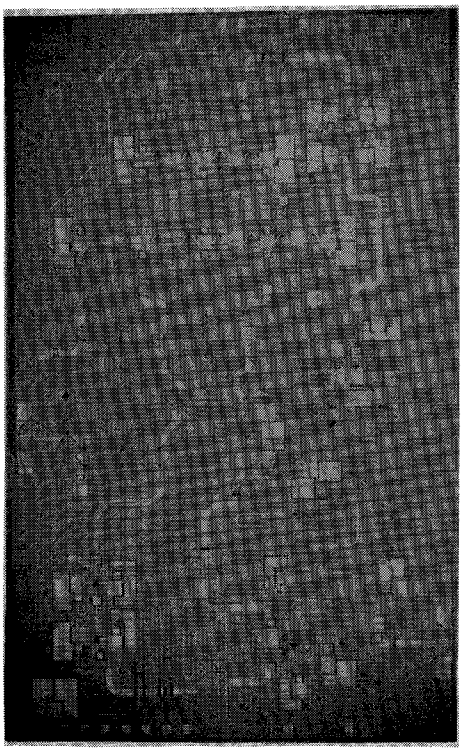

Figure 9: Monolithic Transceiver Circuit.

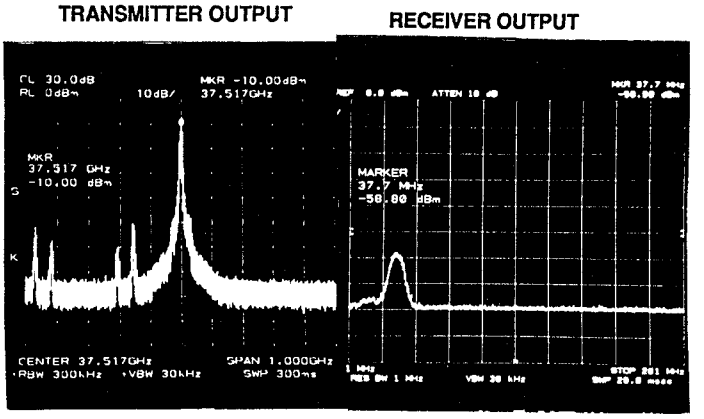

Figure 10: Measured Tranceiver Response.

Conclusion

A monolithic HEMT transceiver has been described. This circuit demonstrates the benefit of InGaAs HEMT technology to simultaneously provide both low noise and medium power circuits using single process technology. Based on the size of the chip and the performance, it clearly illustrates the advantages of MMICs in system applications, namely smaller size weight, and potential cost savings.

Acknowledgements

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References

[1] J. Berenz, et al, "44 GHz Monolithic Low Noise Amplifier," IEEE MMMCS Digest, Las Vegas, NV, June 1987, pp. 15 - 17.

[2] J. Berenz, M. LaCon, M. Aust, "44 GHz Monolithic HEMT Downconverter," 1990 IEEE GaAs IC Symposium Technical Digest, October 1990, pp. 189 - 193.